A 12-bit CIFF Noise Shaping ADC for Neural Recording

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ABSTRACT

This work presents a 2nd order tri-level quantizer based delta sigma(ΔΣ) modulator for neural recording. The modulator implements structure of feed forward form of Cascade Integrator feedback (CIFF) for power reduction even one extra operational amplifier is utilized for the adder. The modulator Signal Transfer Function (STF) shows a low-pass response. While the Noise Transfer Function (NTF) shows the high pass response, to shapes the quantization noise at higher frequencies. The NTF with zero optimization technique results in Signal to Noise Ratio (SNR) of 75 dB, while without NTF zero optimization technique SNR of 67dB. Due to relax requirement of the Out of Band Gain (OBG) is 1.5. The zeroes and poles of the NTF discussed. The poles lie inside the unit circle while zeroes lie on the unit circle. Operational amplifier for integrator optimized for much lower DC gain, limited slew-rate. The operational amplifier circuit architecture also investigated for higher performance as the system level simulation show relax DC gain requirement. Due to non-idealities of circuit level implementation, thermal noise and flicker noise needs to be modeled and simulated in the MATLAB. The proposed second-order tri-level quantizer delta sigma modulator can achieve 75 dB SNR with an oversampling ration (OSR) of 64 can achieve with full-scale input of 750 mV.

Keywords: DC Gain, Noise transfer function, Signal transfer function, Thermal noise, Operational amplifier

1. INTRODUCTION

A 2nd order tri-level delta sigma(ΔΣ) modulator modeled and simulated for neural recording applications. The modulator can achieve 12-bit resolution with an oversampling ratio of 64. The complete modulator modeled simulation of system level for circuit non-idealities like limited DC gain. A power-efficient complementary metal oxide semiconductor neural signal-recording readout circuit for multichannel neuromodulation implants is given in this work. The system includes a neural amplifier and a Successive Approximation Register (SAR) Analog to Digital Converter (ADC) for digitizing and recording neural signal data to transmit to a remote receiver. By using a LabVIEW myDAQ device the synthetic neural signals are generated and processed with a LabVIEW Graphic User Interface. Standard 0.5 m CMOS technology is used to build the reading circuit. The suggested amplifier used a fully differential design with a reconfigurable capacitive resistive feedback network. To record local field potentials (LFPs) the amplifier achieves 49.26 dB gain with the frequency bandwidth of 0.57-301 Hz and for action potentials (APs), the amplifier achieves 60.53 dB gain within frequency bandwidths of 0.27–12.9 kHz, respectively. By lowering the Noise-Efficiency-Factor (NEF) to 2.53, the amplifier retains a noise–power tradeoff. The common-centroid placement approach is used to manually lay out the capacitors, improving the ADC's linearity.

With an SNR of 45.8 dB and an 8-bit resolution, the SAR-ADC achieves a Signal to Noise Ratio (SNR). At a modest sampling rate of 10k samples/s, the ADC shows an Effective Number of Bits (ENOB) of 7.32. The chip's overall power consumption is 26.02 W, making it ideal for a multi-channel brain signal recording device [1]. Because of stringent dynamic range requirements to resolve small-signal amplitudes buried in noise amidst large artefact and stimulation transients, as well as stringent power and volume constraints to enable minimally invasive untethered operation, neural electrical potentials from the brain pose significant challenges. We describe a neural recording System of sixteen channel on Chip (SoC) in a 65-nm CMOS based process with a higher than input dynamic range of 90 dB and input less than 1 V rms referred noise from dc to 500 Hz, power consumption 0.8W, and 0.024 mm^2 area per channel, with a 0.8 W power consumption and 0.024 mm 2 area per channel. Each recording channel is equipped with a hybrid analog digital second order oversampling ADC. Also, in the digital domain for high conversion gain and dynamic offset subtraction it has biopotential signal connecting directly to the second integrator. To avoid signal distortion, it bypasses the need for filtering based on high pass pre-amplification in neural recording systems. The integrated ADC-direct neural recording offers a record figure of merit, with a combined front end and ADC noise efficiency factor NEF of 1.81 and a matching power-efficiency-factor (PEF) of 2.6. The predictive digital auto-ranging of the binary quantizer allows for even faster transient recovery while staying fully dc-coupled. As a result, the neural ADC can record slow potentials of frequency 0.01-Hz and recover from 200-mV peak-to-peak transients in 1 ms, as both are the key needs for recording based on electrocortical for brain activity mapping. In vivo recordings from the frontal cortex of a marmoset primate show that it has a unique ability to resolve local field potentials which are ultra-slow indicative of the subject's arousal state [2]. This study describes a low noise analogue-front- end (AFE) and a low power analog to digital converter as part of a low noise neural recording integrated circuit (ADC). The biopotentials AFE amplifies, while the ADC is used to convert the input signal to output which is in digital form. The AFE has a -3dB 38.8Hz-10.6kHz of bandwidth with 53.4dB of mid-band gain. AFE has a NEF of 8.1 and 10.8Vrms of total IRN. The ADC has a resolution of 10 bits and runs at 2.5MS/s. In a 0.18m CMOS process, the device is produced and successfully tested. [3].

This paper proposed a second-order tri-level quantizer based delta sigma(ΔΣ) modulator for neural recording. The modulator implements structure of cascade of integrator with multiple feedback (CIFF) for power reduction even one extra operational amplifier is utilized for the adder. The modulator signal transfer function (STF) shows a low-pass response. While the noise transfer function (NTF) shows the high pass response, to shapes the quantization noise at higher frequencies. The NTF zero optimization technique results in signa-to-noise-ratio (SNR) of 75 dB, while without NTF zero optimization technique SNR is 67 dB. Due to relax requirement the OBG set to 1.5. The zeroes and poles of the NTF discussed. The poles lie inside the unit circle while zeroes lie on the unit circle. The operational amplifier for the integrator optimized for much lower DC gain, limited slew-rate. The operational amplifier circuit architecture also investigated for higher performance as the

system level simulation show relax DC gain requirement. Due to non-idealities of circuit level implementation, thermal noise and flicker noise needs to be modeled and simulated in the MATLAB. The proposed second-order tri-level quantizer delta-sigma modulator can achieve SNR of 75 dB with an oversampling ration (OSR) of 64 can achieve with full-scale input of 750 mV.

After the introduction, the second section discuss the design of the modulator design with CIFB and CIFF structure, while the third section describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the fifth-order 4-bit quantizer for CT

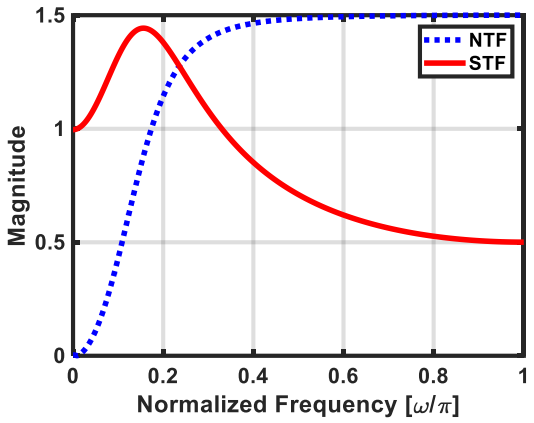

Figure 1: STF and NTF plot (CIFF)

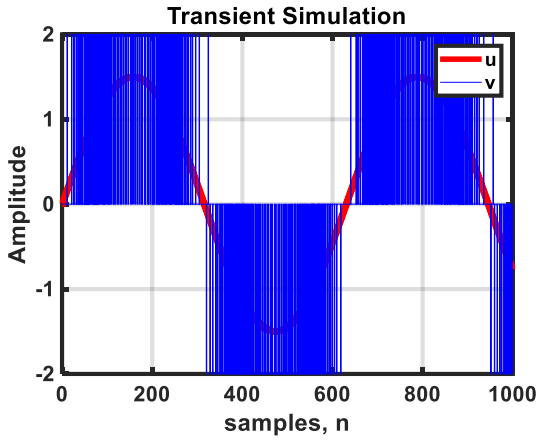

Figure 2: Transient output (CIFF)

design implementation. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A second order with two integrators in the loopfilter and tri-level quantizer modulator modeled using Delta-Sigma Toolbox [12]. The CIFF investigated for higher out-of-band-gain (OBG) of 6 with moderate oversampling ratio of 64 without NTF zero optimization technique. The modulator with CIFB topology can achieve SNR of 75 dB with OSR of 64. Due to the reason of low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency. The coefficients of the proposed second order multiple bit CIFF obtained from Delta-Sigma Toolbox. These coefficients represent the ratio of capacitors at the discrete-time implementation of the modulator. Figure 1 illustrates the modulator's STF and NTF. In Figure 1 it is shown clearly that the OBG of the CIFF modulator is 1.5. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal. The peaking in the STF is due to the CIFF topology. Figure 2 illustrates the modulator's transient output, which demonstrates pulse coded modulation (PCM). Figure 3 depicts the STF and NTF plots. While the Figure 4 shows the output power spectral density (PSD) plot with SNR of 75.6, achieving effective number of bit (ENOB) of 12-bit. The modulator NTF shows a sharp noise shaping response due to the reason that all integrator inside the loopfilter is assumed having infinite DC gain. The noise floor is at the level of -100dB, the quantization noise is suppressed maximum with nine integrators inside the loopfilter. Due to moderate OSR of 64, the signal bandwidth is small. Due to CIFF topology of the

modulator the signal swing inside the loopfilter is smaller as a results operational amplifier with very low DC gain will be demanded for the suppression of the quantization noise. Due to CIFF topology the stability of the loopfilter is very compromised due to the disadvantage of single feedbacks, while the overall modulator becomes power low power with many low DC gain amplifier inside the loopfilter.

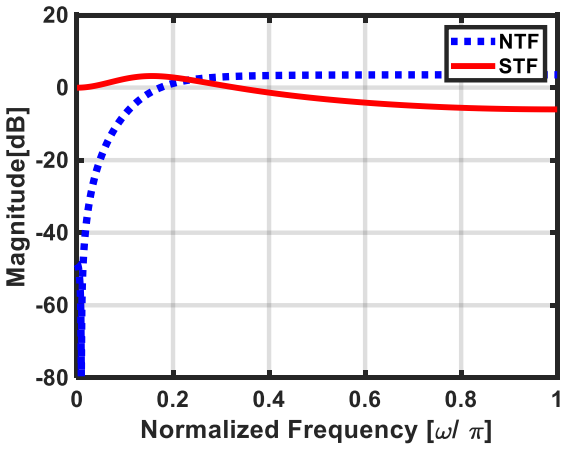

Figure 3: STF and NTF plot (CIFF)

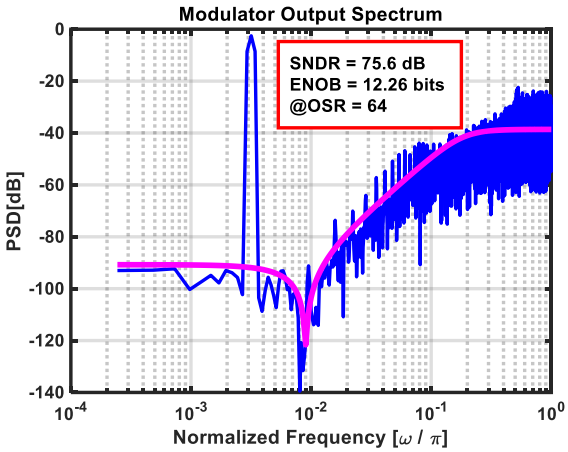

Figure 4: Output PSD plot (CIFF)

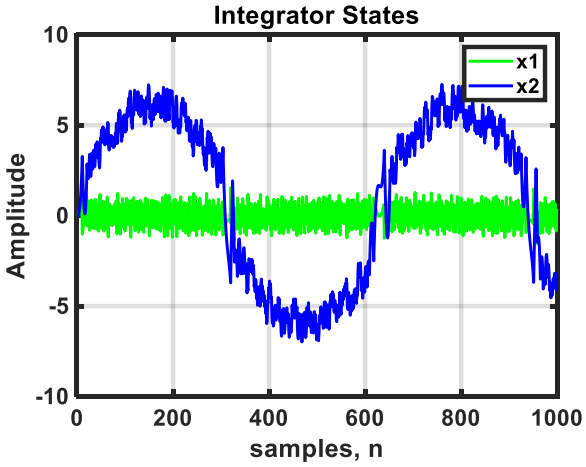

Figure 5: Output states of the integrators

3. RESULTS & DICUSSION

A 2nd order tri-level delta sigma modulator modeled for neural recording applications. The modulator topology is CIFF used for low DC gain requirement, as the loopfilter process only the quantization noise and signal are feedforward to the quantizer. The simulation environment SD Toolbox [14] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

A 2nd order tri-level delta sigma(ΔΣ) modulator is modeled. In simulation, the modulator achieved higher SNR of 75 dB for neural recording application. The NTF zero optimization technique results in signa-to-noise-ratio (SNR) of 75 dB, while without NTF zero optimization technique SNR is 67 dB. Due to relax requirement the OBG set to 1.5. The zeroes and poles of the NTF discussed. The poles lie inside the unit circle while zeroes lie on the unit circle. The operational amplifier for integrator optimized for much lower DC gain, limited slew-rate. The operational amplifier circuit architecture also investigated for higher performance as the system level simulation show relax DC gain requirement. Due to non-idealities of

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5. ACKNOWLEDGMENT

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